Notable Speakers

1. **Prof. (Dr.) P. K. Meher**
   Professor, NTU, Singapore
2. **Prof. (Dr.) C. K. Sarkar**
   Professor, Jadavpur University, Kolkata
3. **Prof. (Dr.) D. P. Acharya**
   Professor, NIT, Rourkela
4. **Prof. (Dr.) A. K. Panda**
   Professor, NIST, Berhampur
5. **Prof. (Dr.) A. Sarkar**
   Professor, Kalyani University, West Bengal
6. **Prof. (Dr.) P. K. Rout**
   Professor, SIT, Bhubaneswar

For any other Enquiry contact:

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Cell :9437284114
Email.sanjit.swain@gmail.com

Contact Address

Dept. of Electronics & Communication Engineering
Silicon Institute of Technology
Silicon Hills, Patia, Bhubaneswar-751024

Registration Form

IEEE EDS Bhubaneswar-Kolkata

Two days National Workshop on Recent Trends in VLSI Devices & Circuits

(RTVDC-2018)

(23rd & 24th February 2018)

Name :
Gender :
Category : (Tick any one) **Student** ☐ **Faculty** ☐ **Others** ☐
Institute Name :
Address for Correspondence : **Phone :** **Mobile :** **E-mail :**
Cash/Draft No :
Amount :
Educational Qualifications :
Highest Degree :
Obtained from :
Subject/Specialization :
University :
Accommodation required : YES / NO **If yes, where : Hostel / Guest House**
Forwarding remark of the Head of the Department / Institution: ***Signature (With Seal)***

Silicon
...beyond teaching

Two days National Workshop on Recent Trends in VLSI Devices & Circuits

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(23rd & 24th February 2018)

Organized by

The Departments of
Electronics & Communication Engg.
and
Applied Electronics & Instrumentation Engg.

in association with

IEEE EDS Bhubaneswar-Kolkata Chapter

Silicon Institute of Technology
Silicon Hills, Patia, Bhubaneswar
Odisha-751024

Overview

The convergence of technology with modern life has reached a state where reliance of human life on semiconductor technology is indispensable and ubiquitous. Today semiconductor technology including non CMOS devices applied in circuits and systems is poised to look beyond its traditional bastions of application with pervasive impact on transportation, energy, disaster management, environment and healthcare.

However in the last few decades due to continuous scaling, several deleterious short-channel effects (SCEs) became prominent and started deteriorating the performance of traditional planar bulk MOSFETs. Hence various non-planar multiple-gate device structures have been proposed in recent years in order to improve the electrostatic control of the channel and to improve the performances of the devices. The basic objective of this workshop is to be familiar with the recent development in Nano scale devices and their application in circuits to face the challenges in future in the analog/RF applications and also to provide solutions for the low-power VLSI IC design.

Topics

- Concepts of advanced MOSFETs
- Tools Related to advanced MOSFET
- Simulated tutorials on advanced MOSFET Using TCAD
- Hetero-Structure based Nano- scale MOSFETs
- Advanced MOSFET for RF Applications, Advances in CMOS based nonvolatile memories
- Advances in CMOS mixed signal circuits
  Voltage controlled oscillator (VCO)
  Phase Locked Loop (PLL)
  Analog to Digital Converter (ADC)

Venue

Silicon Institute of Technology, Patia, Bhubaneswar-751024

Silicon Institute of Technology (SIT) was established in the year 2001 in the temple city Bhubaneswar, Odisha with a vision to provide value-based quality education. The institute is recognized as one of the centers of academic excellence and vibrant research culture in the state and outside. Over the years, Silicon institute has been recognized as one of the premier technological institutes both in academics and research in the state of Odisha and India. The campus is easily accessible and approximately 13 kms away from the Railway Station and 16 kms away from Biju Patnaik Airport, Bhubaneswar.

Registration Fees

External Faculty and
Industry Professionals : ₹ 1200/-
External/ Internal Students : ₹ 600/-
IEEE, ISTE student members : ₹ 500/-

Registration Information

Participants can register by sending the registration form along with demand draft (appropriate amount) in favor of Silicon Institute of Technology, payable at Bhubaneswar. Students have to submit bonafide certificates from the Heads of their Institutions along with the registration forms on or before 20th February 2018.

Provision for Poster Presentation

Interested participants are invited to present their work in the form of poster (A1 size) and are requested to give their consent before 20th February 2018 to the Program Coordinators.

(The best three student presentations will be awarded with cash prizes)

Accommodations

Limited Accommodation is available at the Institute Guest house at concessional rates on first-come-first serve basis.

Chief Patron

Prof. (Dr.) S. K. Misra
Director, SIT, Bhubaneswar

Advisory Committee

Prof. (Dr.) J. Talukdar, Principal

Prof. (Dr.) B. B. Misra, Dean(Research)

Prof. (Dr.) D. Kar, Dean(Academics)

Prof. (Dr.) P. K. Rout, HOD(AE&I)

Prof. (Dr.) S. K. Pati, HOD(ECE)

Convener

Prof. Sanjit Kumar Swain
Dept. of ECE., SIT, Bhubaneswar

Program Coordinator

Prof. Umakanta Nanda
Dept. of ECE, SIT, Bhubaneswar

Prof. Sudhansu Mohan Biswal
Dept. of AEI, SIT, Bhubaneswar

Organizing Committee

Staff of the Departments of
Electronics & Communication Engg.
&
Applied Electronics & Instrumentation Engg.